SOCIETY FOR ELECTRONIC TRANSACTIONS AND SECURITY [SETS]

Operational Headquarters

CIT Campus, MGR Knowledge City, Taramani, Chennai – 600 113. India.

Website: **www.setsindia.org**

Society for Electronic Transactions and Security [SETS] is a non-profit society dedicated to research and development in the field of Information Security. SETS has been registered as a Society under Societies Registration Act, XXI of 1860 Registration No.S42605 of 2002 with Registrar of Societies New Delhi. It was formed as a Government of India initiative under the office of Principal Scientific Advisor (PSA) to GoI.

Applications are invited from the Indian nationals for the position of Project Associate to work in the field of Hardware Security in the project entitled **"**Physical Unclonable Function (PUF) based Application Specific IC (ASIC) by Technology-Circuit-System Co-Development for Strategic Applications**"** funded by the office of PSA. **The positions as proposed are purely temporary and would be filled on Contract basis with consolidated salary under the project. The project has Proposed Date of Completion (PDC) of 36 months. The appointment will be made initially for a period of two years and extendable upto further one more year or the closing date of the project whichever is earlier. Thus, the contract shall be co-terminus with the project. However, there is no scope of continuation / regularization / absorption under any circumstances.**

The descriptions of positions, detailed qualifications, skill sets and salary are given below:

Advertisement No	SETS/Chn/Rec/Proj-PUF/2018-19/02
Name of the Post	PROJECT ASSOCIATE
Number of Positions	2
Salary	Rs 40,000 per month - Rs 50,000 per month commensurate to relevant experience
Age Limit	Not more than 35 years as on 10-04-2019
Educational Qualification	M.E/M.Tech in **Electronics and Communication Engineering/ Computer Science and Engineering/ Applied Electronics/ Embedded Systems/ VLSI Design** from a recognized university in First Class with 60% or above marks or equivalent.
Areas of Skill sets/ Knowledge required	a) Knowledge in cryptology and strong background in digital system design, including project development experience in C, MATLAB, VHDL/Verilog programming. b) In-depth knowledge of front end digital design process and related design flows (Xilinx FPGA /ASIC digital IC design). c) Candidates with prior industrial/research experience in the field of Hardware Security including Physical Unclonable Function (PUF) and Side Channel Attacks (SCA) are preferred. d) Candidates having post graduate diploma/ advanced certification in VLSI design from reputed institute/ centre will have added advantage.

Application Procedure:

1. Applications received via email will ONLY be considered. Candidate should write "Application for Project Associate Position" in the subject line of his/her E-mail.
2. The candidate is required to attach the Personal Particulars Form in pdf format duly filled and signed.
3. The email should be sent to hrpuf2019@setsindia.net
4. **The last date for receiving applications by email is April 10, 2019.**
5. Shortlisted candidates would be required to attend a Written Test and/or Interview at SETS, Chennai. The date and time for Written Test and/or Interview would be intimated to shortlisted candidates by email.

Terms and Conditions:

1. The shortlisted candidates would be required to bring all their original testimonials for verification on the Written Test/ interview day.
2. No TA/DA will be given to candidates appearing for written test or interview.
3. The prescribed qualifications are minimum and mere possession of the same does not entitle the candidate to be called for the written test or interview. The decision of the Executive Director of SETS in all matters relating to eligibility, acceptance or rejection of the applications or cancellation of the process altogether will be final and no inquiry or correspondence will be entertained in this matter.

CAAO, SETS